Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**

**Graphical user interface

Description automatically generated**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: FLOAT**

**Mask Ref:**

**APPROVED BY: KW DIE SIZE .039 X .050” DATE: 2/7/23**

**MFG: ZYTREX THICKNESS: ” P/N: 54HCT02**

**DG 10.1.2**

#### Rev B, 7/19/02